

# □ MN101D10F , MN101D10G

Type	MN101D10F	MN101D10G
ROM (x8-bit)	96 K	128 K
RAM (x8-bit)	2.5 K	3.5 K
Package	QFP100-P-1818B *Lead-free	
Minimum Instruction Execution Time	With main clock operated	0.1397 $\mu$ s (at 4.0 V to 5.5 V, 14.32 MHz) 71.5 $\mu$ s (at 2.7 V to 5.5 V fixed to 14.32 MHz internal frequency division)
	When sub-clock operated	61 $\mu$ s (at 2.5 V to 5.5 V, 32.768 kHz)
Interrupts	<ul style="list-style-type: none"> <li>• RESET • Runaway • External 0 • External 1 • External 2 • External 3 • External 4</li> <li>• Timer 0 • Timer 1 • Timer 2 • Timer 3 • Timer 6 • Capstan FG • Control • HSW</li> <li>• Cylinder(Drum) FG • Servo V-sync • Synchronous output • OSD • XDS • Serial 0</li> <li>• Serial 1 • Serial 2 • PWM 4 • OSDV-sync</li> </ul>	
Timer Counter	Timer counter 0: 8-bit x 1 (timer function)	
	Clock source	1/4, 1/16 of system clock frequency
	Interrupt source	overflow of timer counter 0
	Timer counter 1: 8-bit x 1 (timer function, linear timer counter function)	
	Clock source	1/4 of system clock frequency; CTL signal
	Interrupt source	overflow of timer counter 1
Timer Counter	Timer counter 2: 16-bit x 1 (timer function, input capture, duty judgment of CTL signal(VISS/VASS detection function), generation of remote control output carrier frequency)	
	Clock source	1/4, 1/16, 1/24 of system clock frequency
	Interrupt source	overflow of timer counter 2; input of CTL specified edge; underflow of timer 2 shift register 4-bit counter; coincidence of timer 2 shift register with timer 2 shift register compare register
	Timer counter 3: 16-bit x 1 (timer function, generation of serial transmission clock)	
	Clock source	1/4, 1/16 of system clock frequency
	Interrupt source	overflow of timer counter 3
Timer Counter	Timer counter 5: 19-bit x 1 (watchdog, stable oscillation waiting function)	
	Clock source	system clock
	Watchdog interrupt source	1/2 <sup>16</sup> , 1/2 <sup>19</sup> of timer counter 5 frequency
	Clear by stable oscillation	after 256 counts by timer counter 5 (2 <sup>18</sup> counts of OSC oscillation clock)
Timer Counter	Timer counter 6: 16-bit x 1 (clock function [max. 2 s])	
	Clock source	1/512 of OSC oscillation clock frequency; XI oscillation clock; 1/8, 1/128 of system clock frequency
	Interrupt source	1/2 <sup>13</sup> , 1/2 <sup>14</sup> , 1/2 <sup>15</sup> overflow of timer counter 6
Serial Interface	Serial 0: 8-bit x 1 (synchronous type) (transfer direction of MSB/LSB selectable, start condition function)	
	Clock source	1/8, 1/16, 1/32, 1/64, 1/128, 1/256 of system clock frequency; NSBT0 pin input
	Serial 1: 8-bit x 1 (synchronous type/remote control transmission) (transfer direction of MSB/LSB selectable, start condition function)	
	Clock source	1/8, 1/16, 1/32, 1/64, 1/128, 1/256 of system clock frequency; 2-division timer 3 output; NSBT1 pin input
	Remote control clock	2-division timer 3 output
Serial Interface	Serial 2: 8-bit x 1 (I <sup>2</sup> C) (master transmission/reception, slave transmission/reception)	
	Clock source	1/144 to 1/252 of system clock; SCK pin input

<b>OSD</b>	Display mode	:	menu(internal synchronized) display, superimpose(externally synchronized) display
	Applicable broadcasting system	:	NTSC, PAL, PAL-M, PAL-N
	Screen configuration	:	24 characters × 2n rows (n = 1 to 6)
	Character type	:	max. 256 character types (variable, include special characters)
	Character size	:	12 × 18 dots (vertical direction: 1 dot for 2H at not enlargement)
	Enlarged characters	:	each × 2 settings in horizontal and vertical
	Character interpolation	:	none
	Line background color	:	8-hue settable in the row unit at menu display
	Line background intensity	:	8 gradations settable in the row unit
	Screen background color :	:	8-huesettable at menu display
	Character color	:	white
	Character intensity	:	8 gradations settable in the row unit
	Border function	:	1-dot border in 8 directions
	Border brightness	:	4 gradations settable in the row unit
	Blinking	:	none (covered by software)
	Inverted character	:	settable in the character unit
	Halftone	:	none
	Input	:	composite video signal input (output level: 1 V[p-p] / 2 V[p-p])
	Clamp method	:	sync tip clamp, clamp level in 4 levels
	Output	:	composite video output
	Measure against image fluctuation	:	built-in AFC circuit
Dot clock	:	1/2 of OSC oscillation clock (automatic phase adjustment)	
MESECAM compatibility	:	Subcarrier leak function for superimpose display	
<b>XDS</b>	Built-in U.S. closed caption data slicer (optional 1 line data can be extracted.)		
<b>ROM Correction</b>	Correcting address designation: up to 3 addresses possible Correction method: correction program being saved in internal RAM		
<b>I/O Pins</b>	<b>I/O</b>	76	• Common use: 56
	<b>Input</b>	1	• Common use: 1
<b>A/D Inputs</b>	8-bit × 12-ch. (without S/H)		
<b>PWM</b>	13-bit × 2-ch. (at repetition cycle 572 μs at 14.32 MHz), 8-bit × 1-ch. (at repetition cycle 35.7 μs, 0.572 ms, 1.14 ms, 2.29 ms at 14.32 MHz)		
<b>ICR</b>	16-bit × 2-ch.(Speed system), 18-bit × 4-ch.(Phase system)		
<b>OCR</b>	16-bit × 3 (Synchronous output × 2, Rec CTL × 1 )		
<b>Special Ports</b>	3-state output (PTO) VLP pin; CTL input; Capstan FG input; Cylinder(Drum) PG/FG inputs; HSW output; Head amp/ Rotary outputs; built-in FG amp; output of 1/4 OSC oscillation clock (1 V[p-p])		
<b>Notes</b>			

See the next page for electrical characteristics, pin assignment and support tool.

## Electrical Characteristics

### Supply current

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Operating supply current	IDD1	14.32 MHz operation without load, VDD = 5 V		50	100	mA
	IDD2	1/1024 of 14.32 MHz operation without load, VDD = 2.7 V		2	5	mA
	IDD3	Stop of 14.32 MHz oscillation, VDD = 2.7 V 32 kHz oscillation operation without load		50	100	μA
Supply current at STOP	IDSP	Stop of oscillation without load, VDD = 5 V, Ta = 55 °C			10	μA
Supply current at HALT	IDHT0	14.32 MHz oscillation without load, VDD = 5 V		5	15	mA
	IDHT1	Stop of 14.32 MHz oscillation, VDD = 2.7 V 32 kHz oscillation operation without load		5	20	μA

(Ta = 25 °C ± 2 °C, VSS = 0 V)

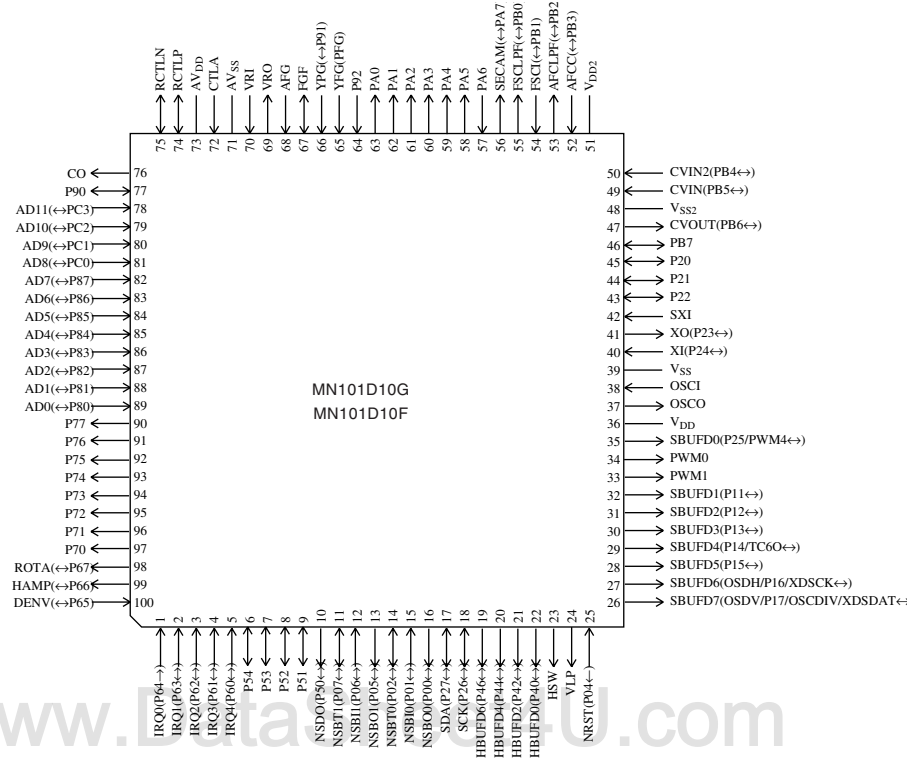
### A/D Converter Performance

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
Conversion relative error	ΔNLAD				± 3	LSB
A/D Conversion Time	tAD	fosc = 14.32 MHz		8		μs
Analog Input Voltage					5	V

(Ta = 25 °C ± 2 °C, VDD = 5.0 V, VSS = 0 V)

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## Pin Assignment



QFP100-P-1818B \*Lead-free

## Support Tool

<b>In-circuit Emulator</b>	PX-ICE101C / D + PX-PRB101D10-QFP100-P-1818B-CN-M	
<b>Flash Memory Built-in Type</b>	Type	MN101DF10GAF
	ROM (× 8-bit)	128 K
	RAM (× 8-bit)	4 K
	Minimum instruction execution time	0.1397 μs (at 4.0 V to 5.5 V, 14.32 MHz) 71.5 μs (at 2.7 V to 5.5 V, fixed to 14.32 MHz internal division) 61 μs (at 2.5 V to 5.5 V, 32.768 kHz)
	Package	QFP100-P-1818B *Lead-free

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